

FIG. 2

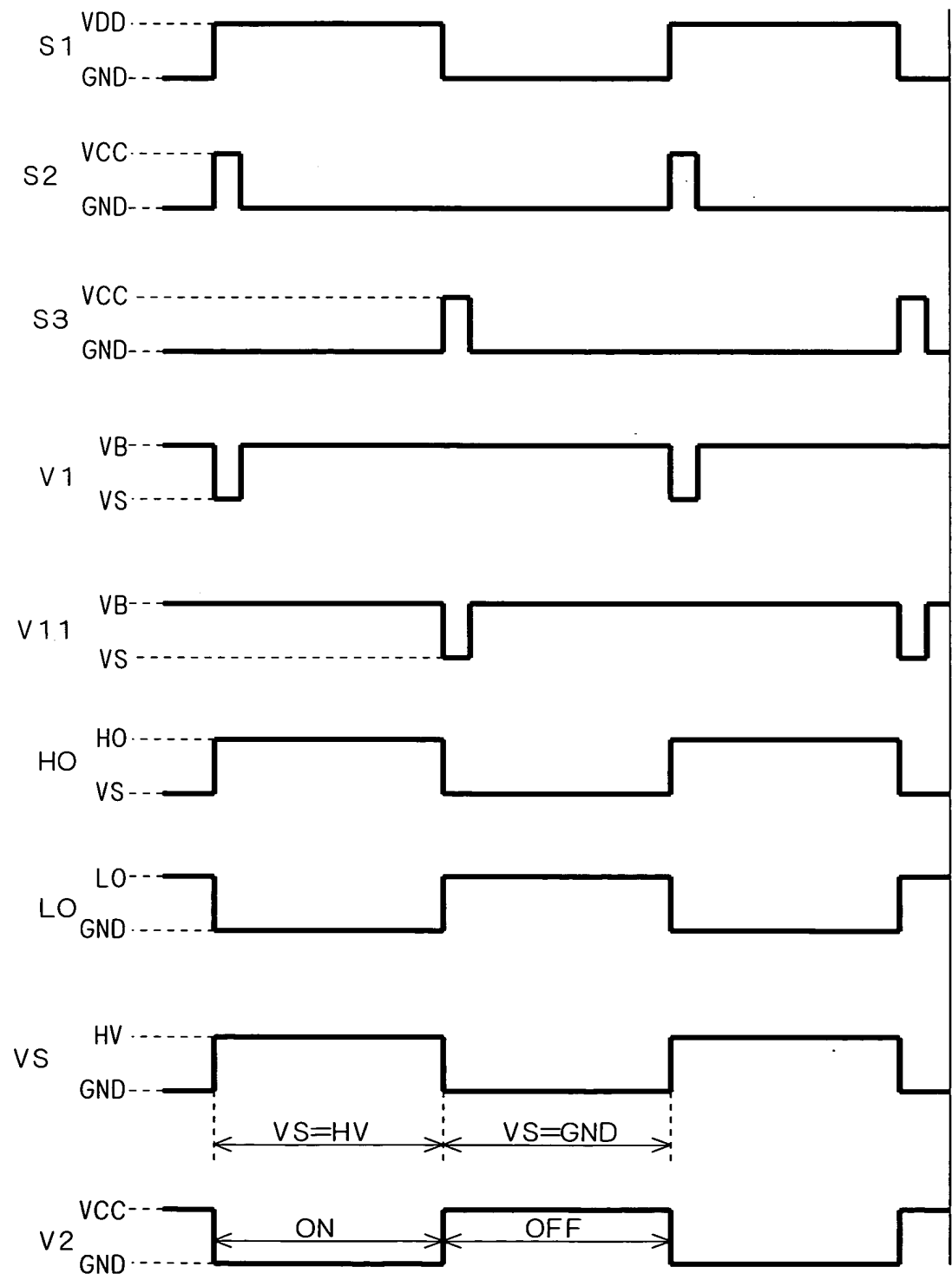


FIG. 3

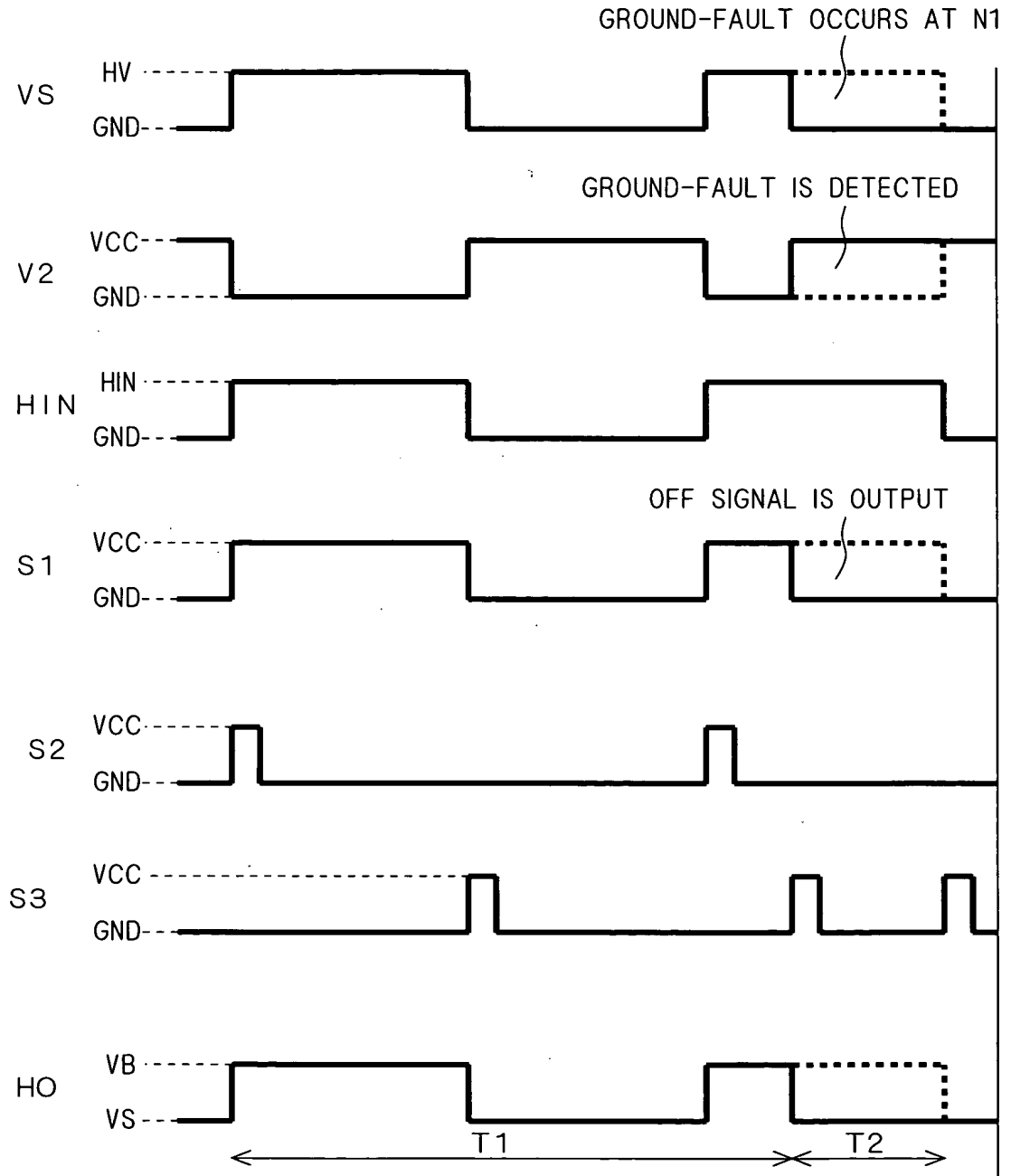


FIG. 4

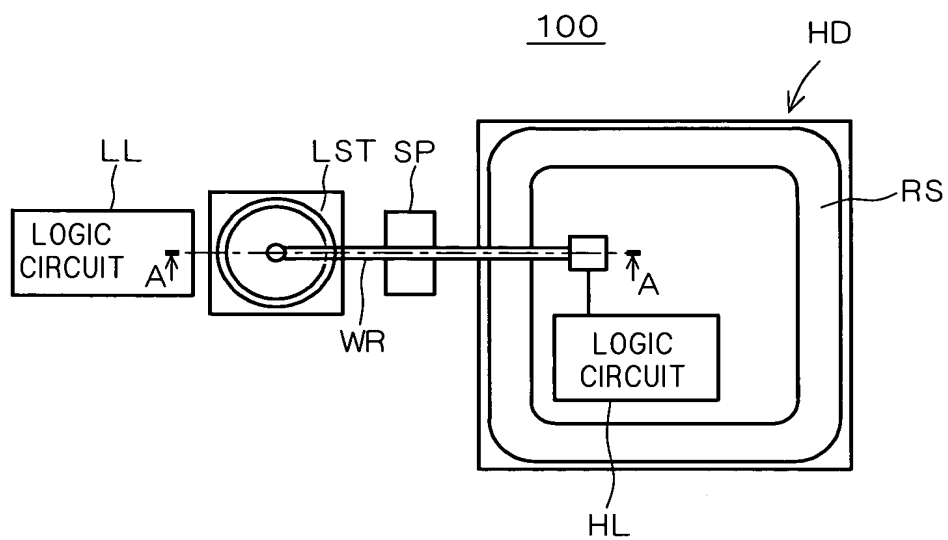


FIG. 5

100

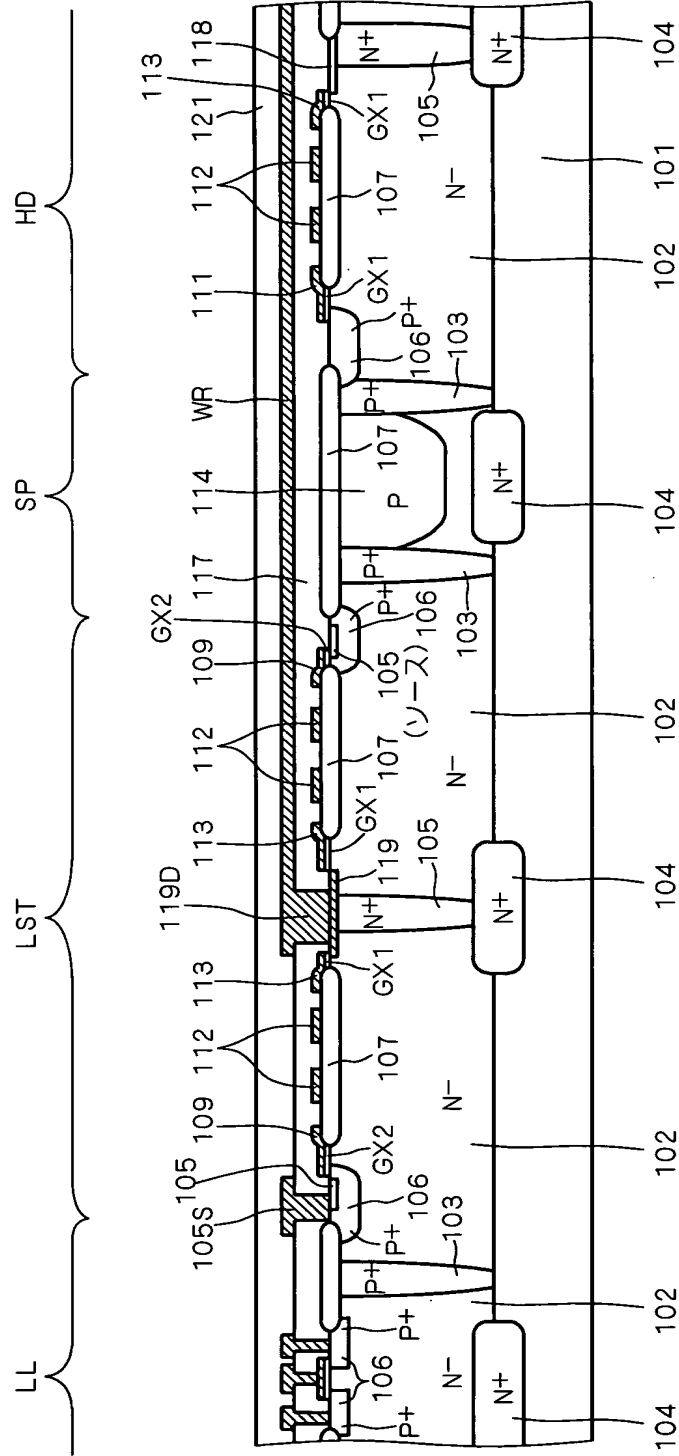


FIG. 6

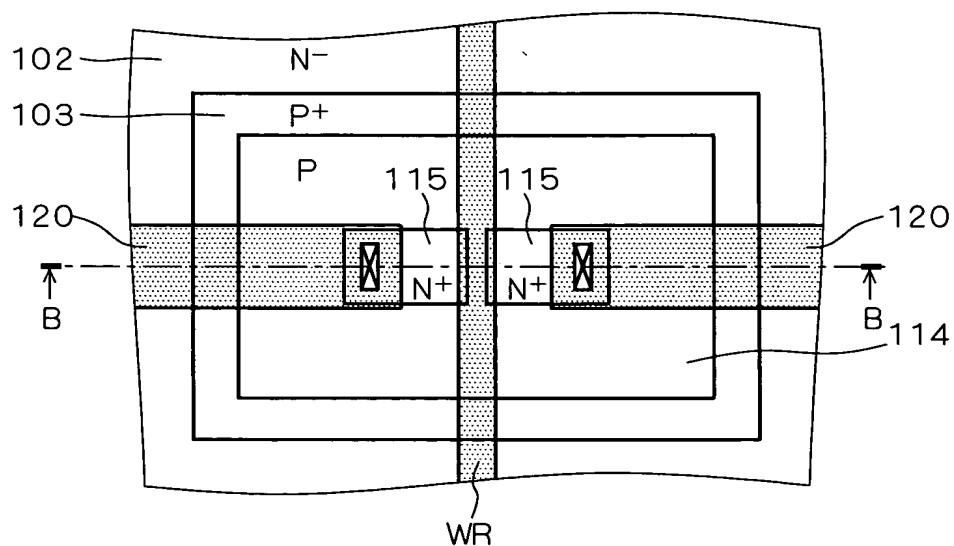
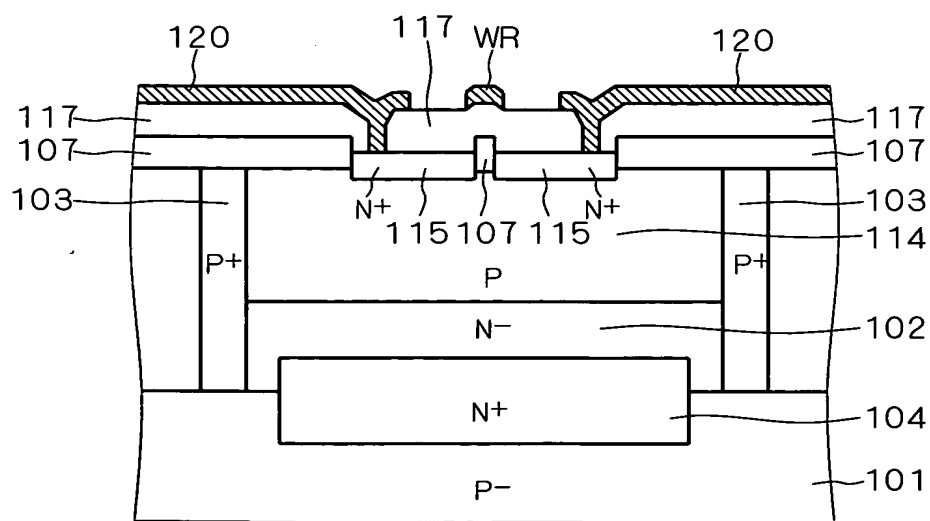
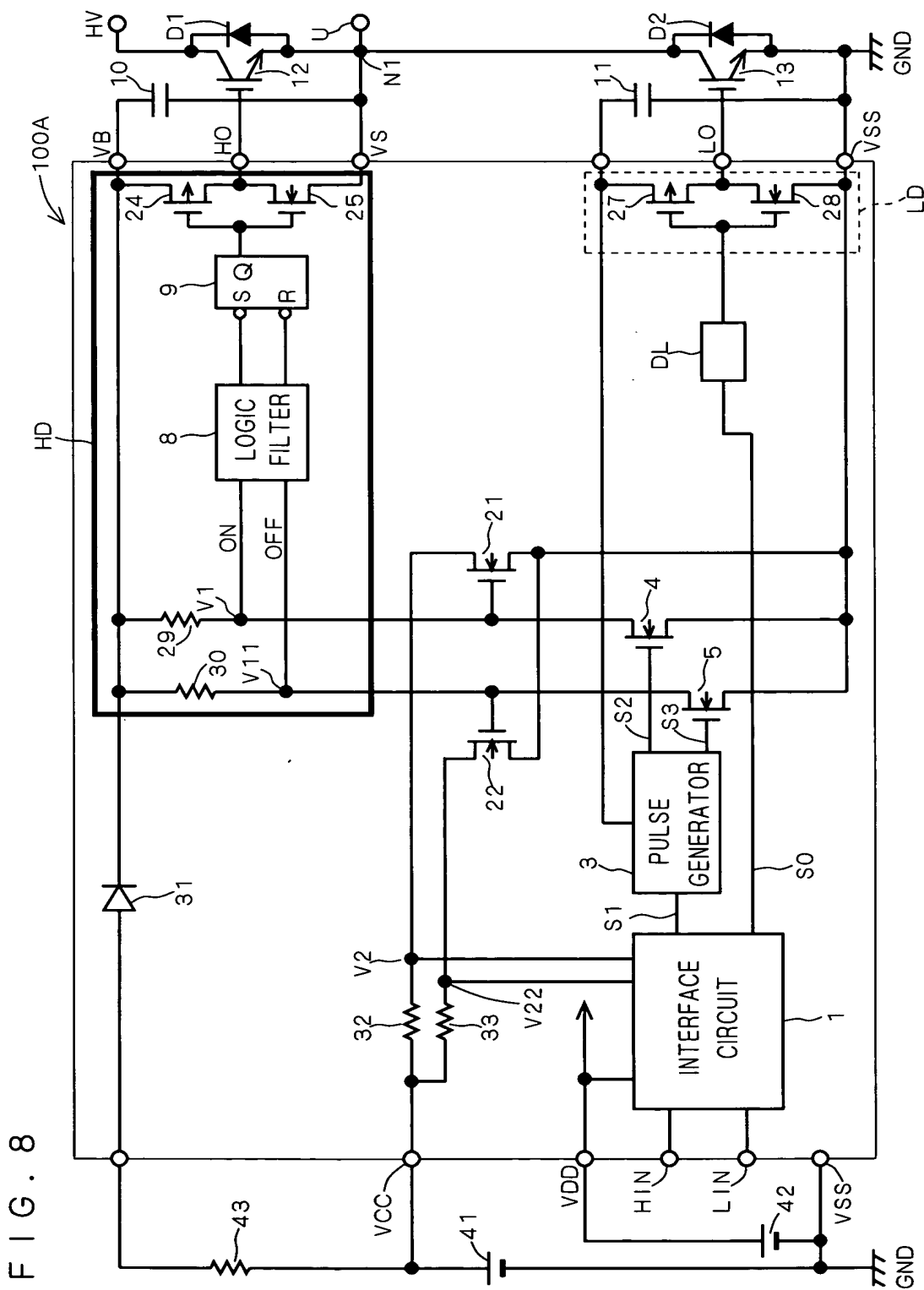


FIG. 7





F I G . 9

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

FIG. 10

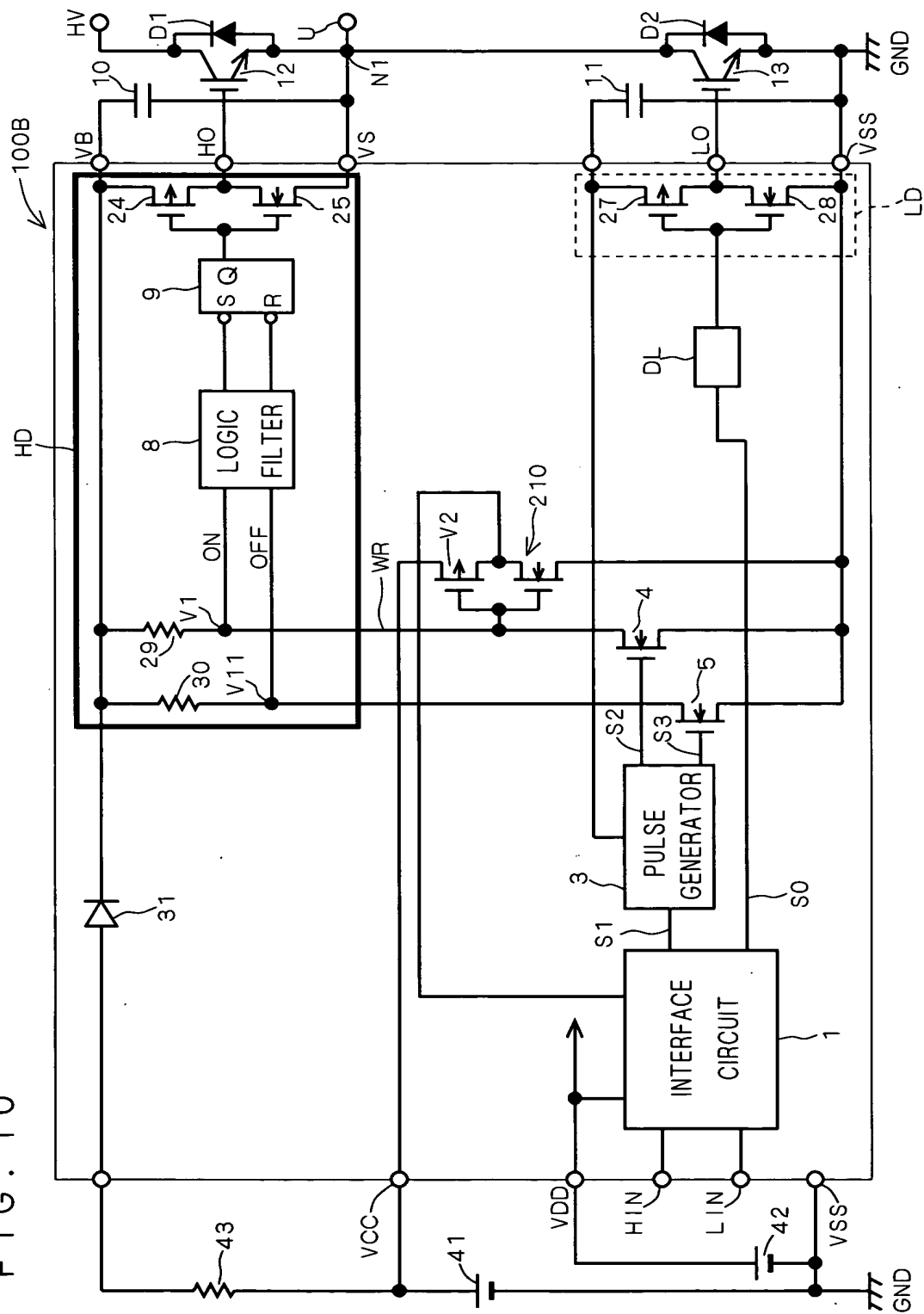


FIG. 12

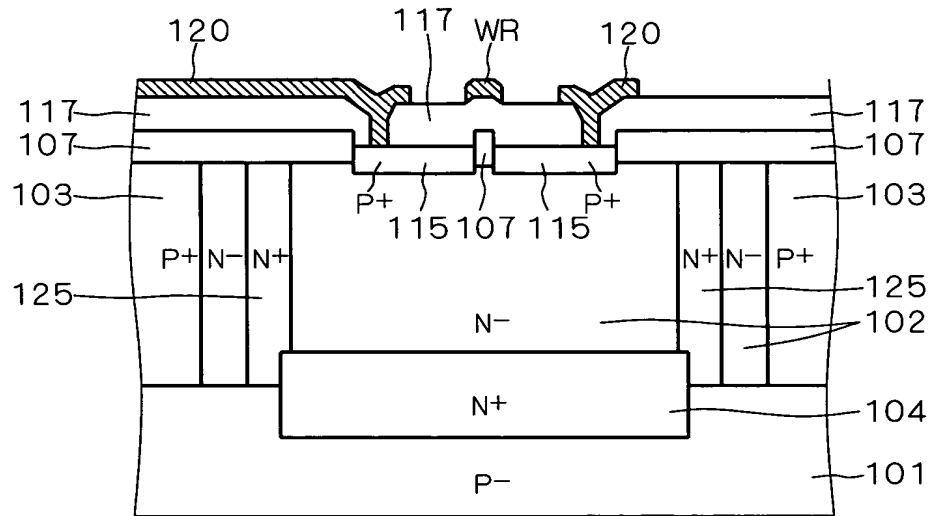


FIG. 13

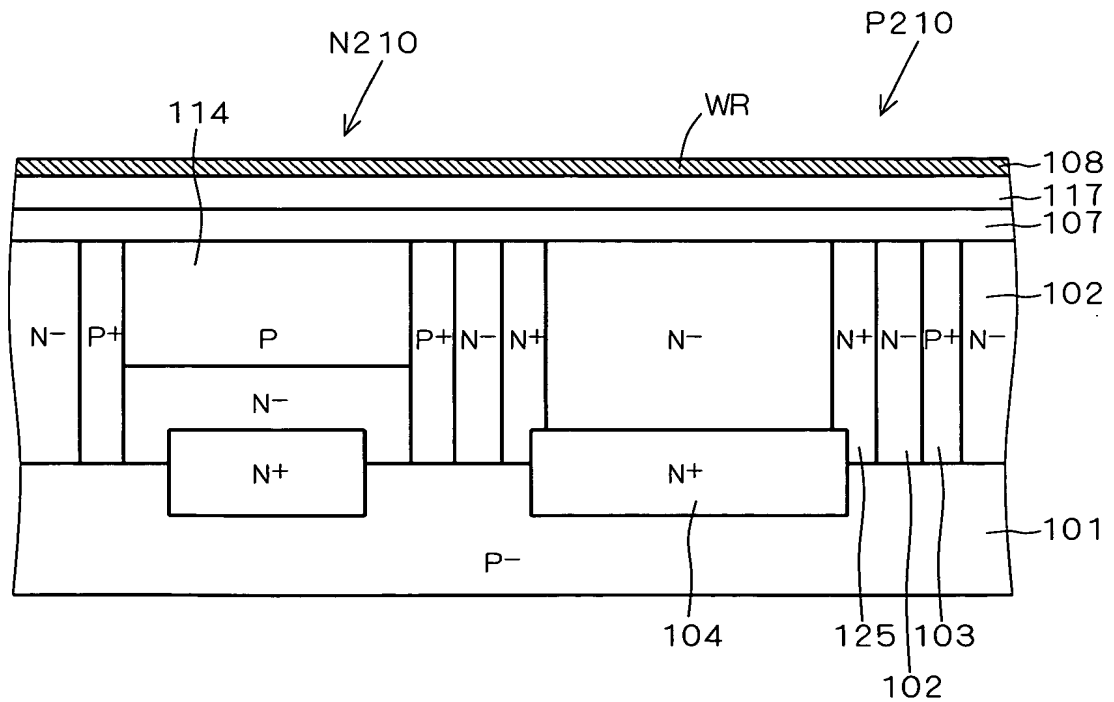


FIG. 14

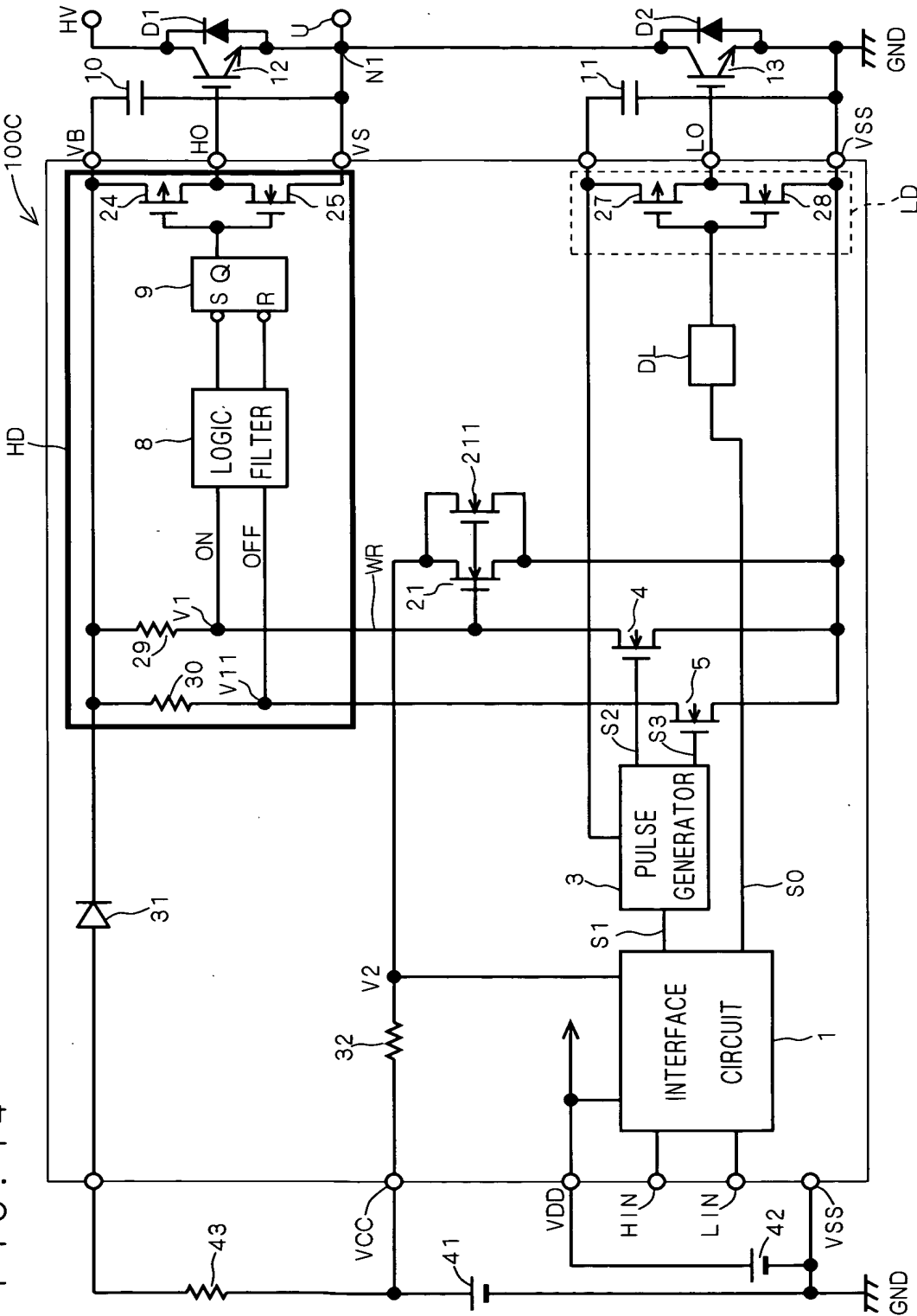


FIG. 16

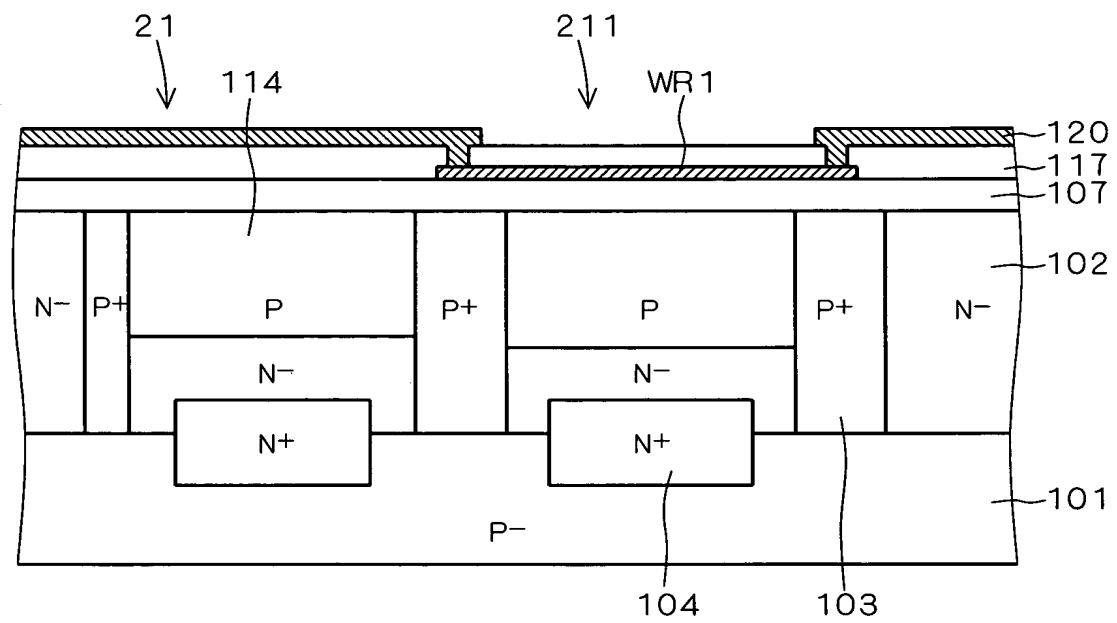


FIG. 17

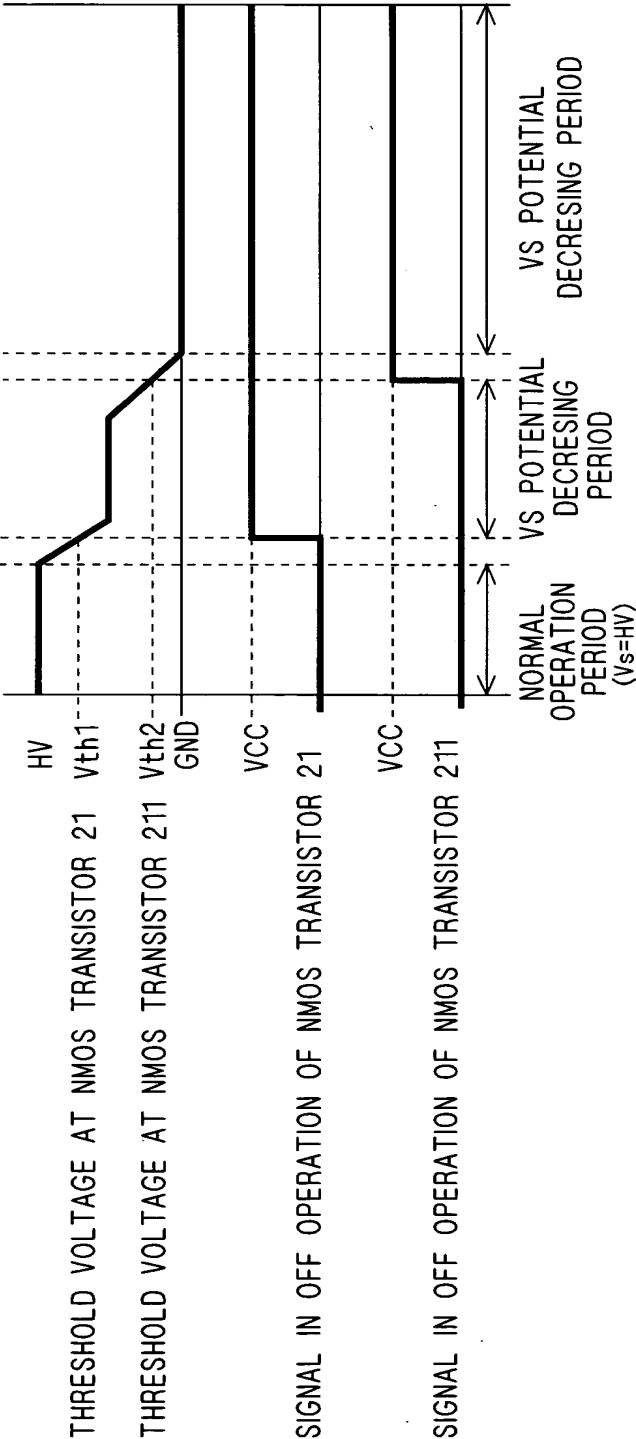


FIG. 18

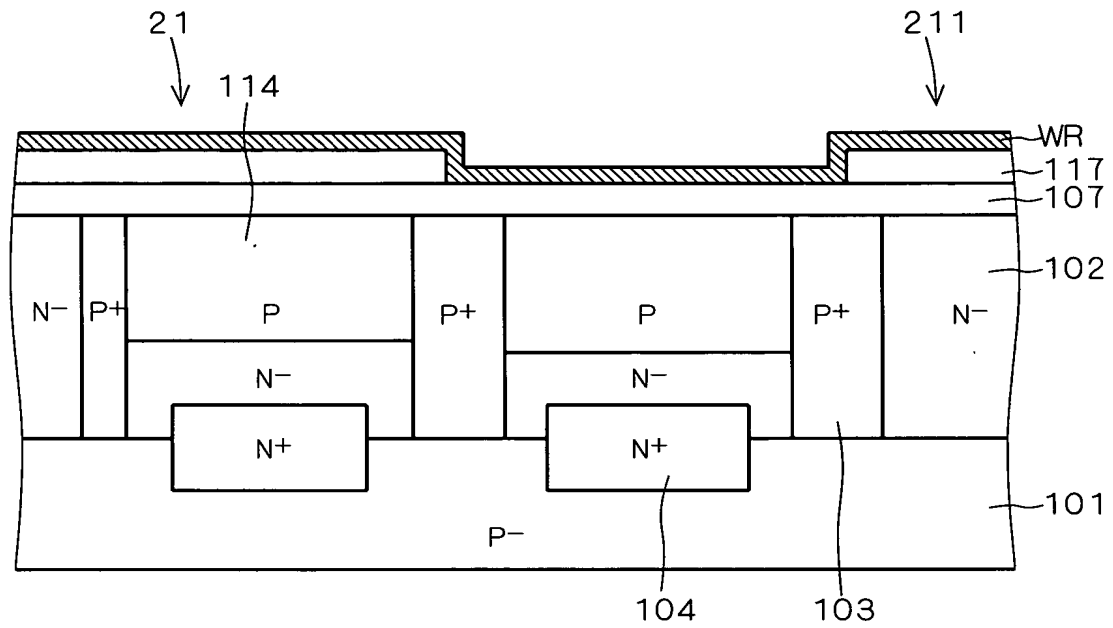
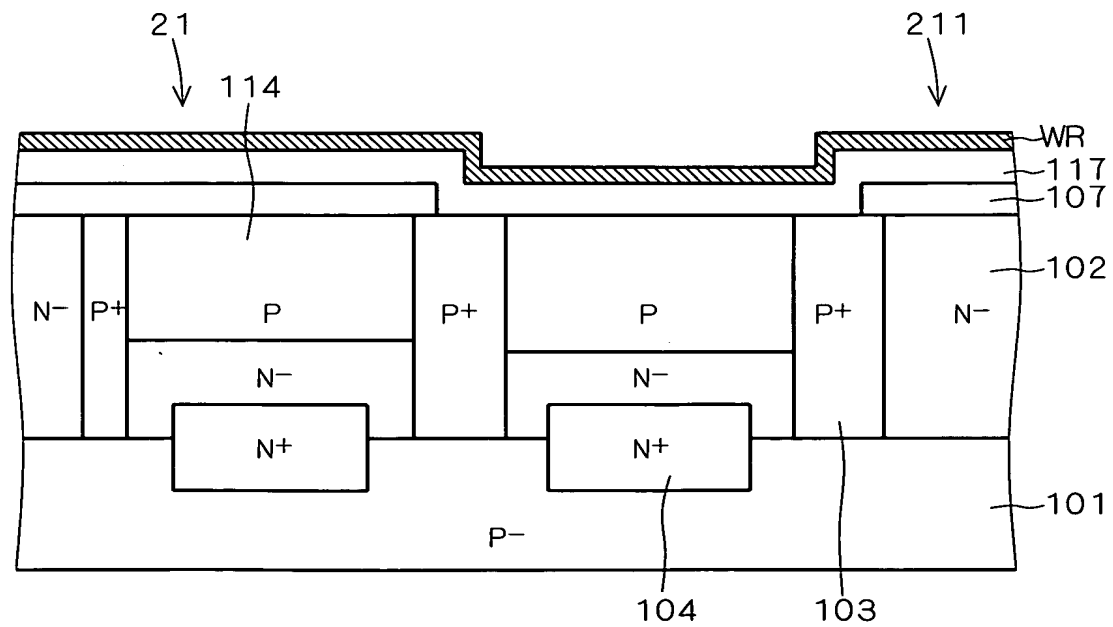


FIG. 19



F I G . 20

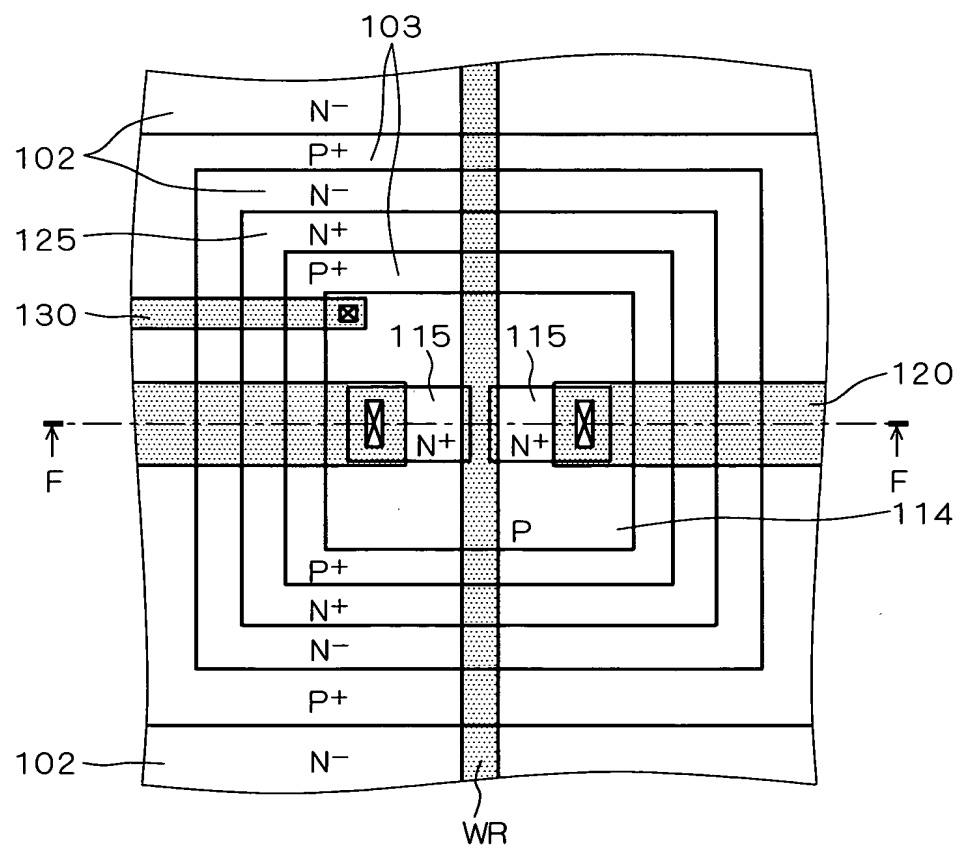


FIG. 21

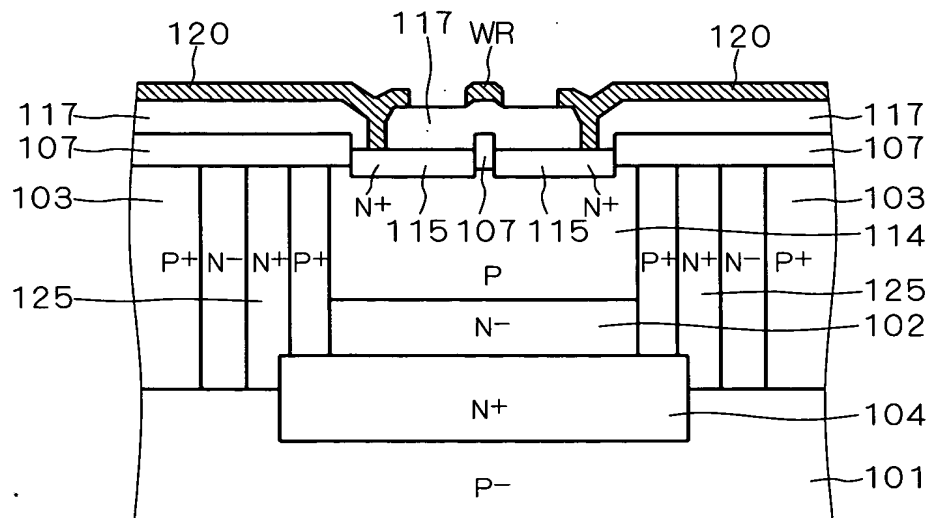


FIG. 22

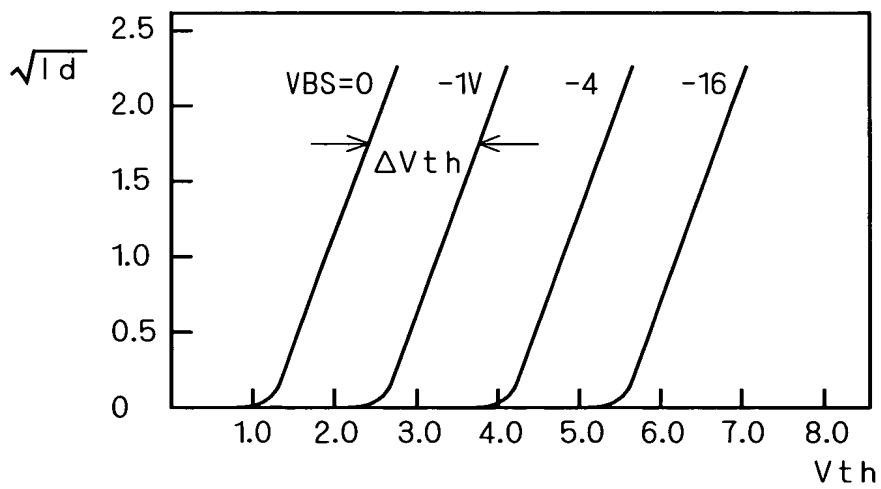
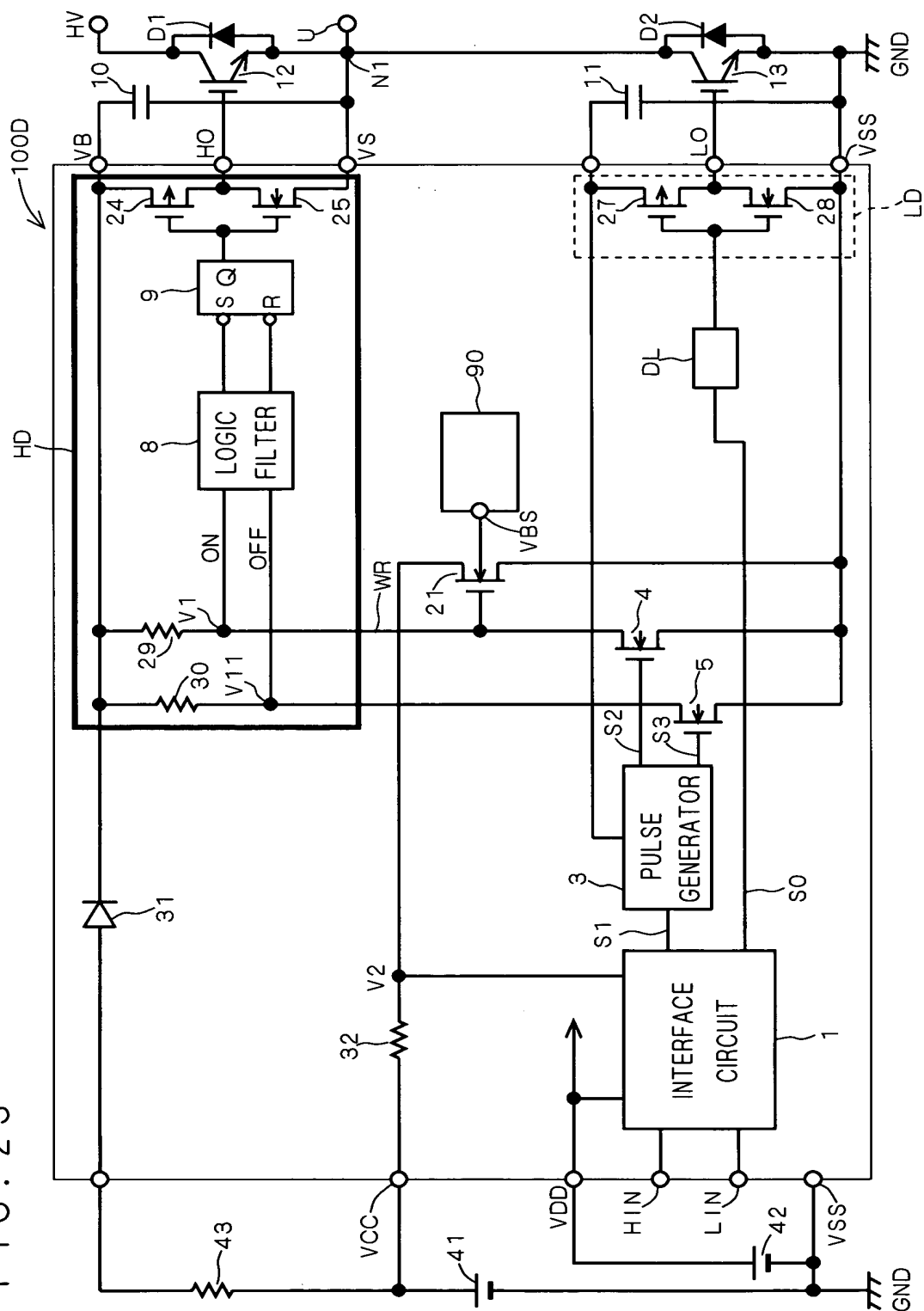


FIG. 23



F I G . 2 4

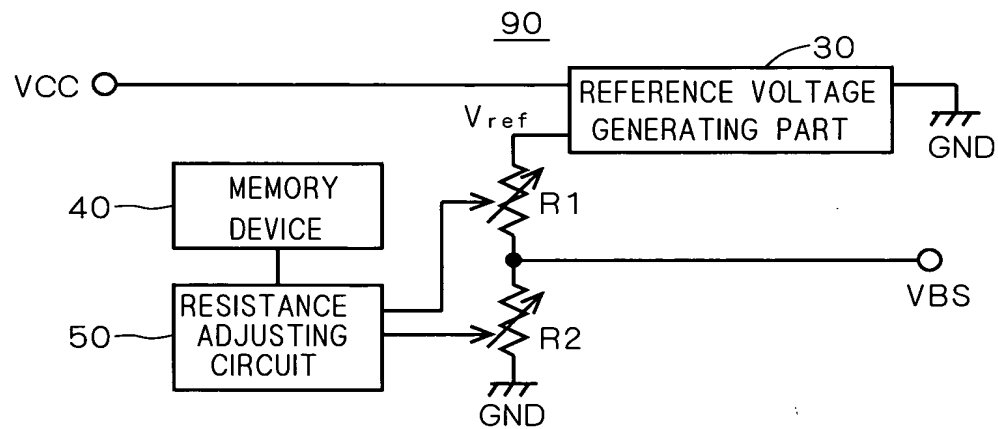


FIG. 26

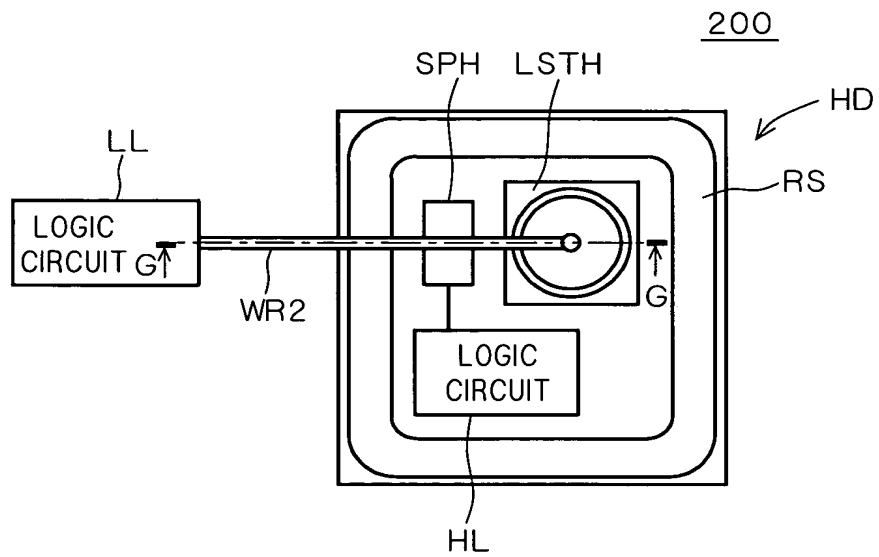


FIG. 27

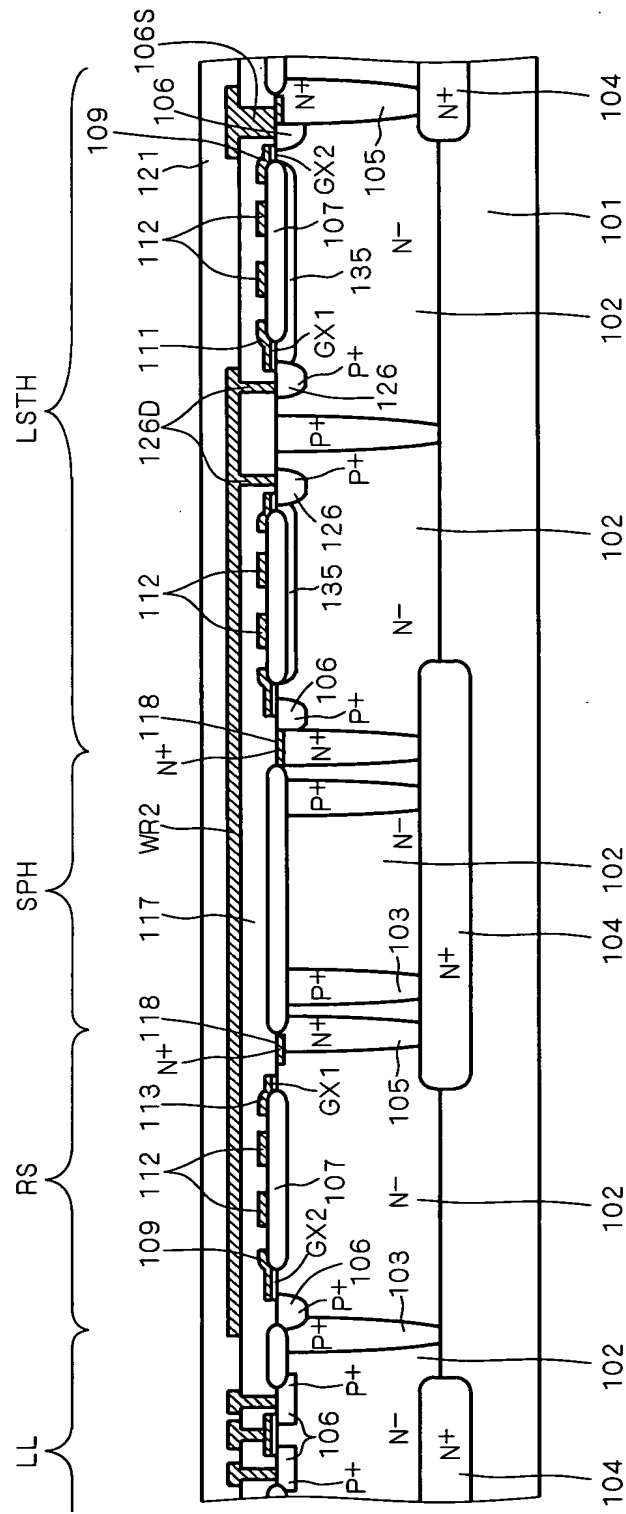


FIG. 28

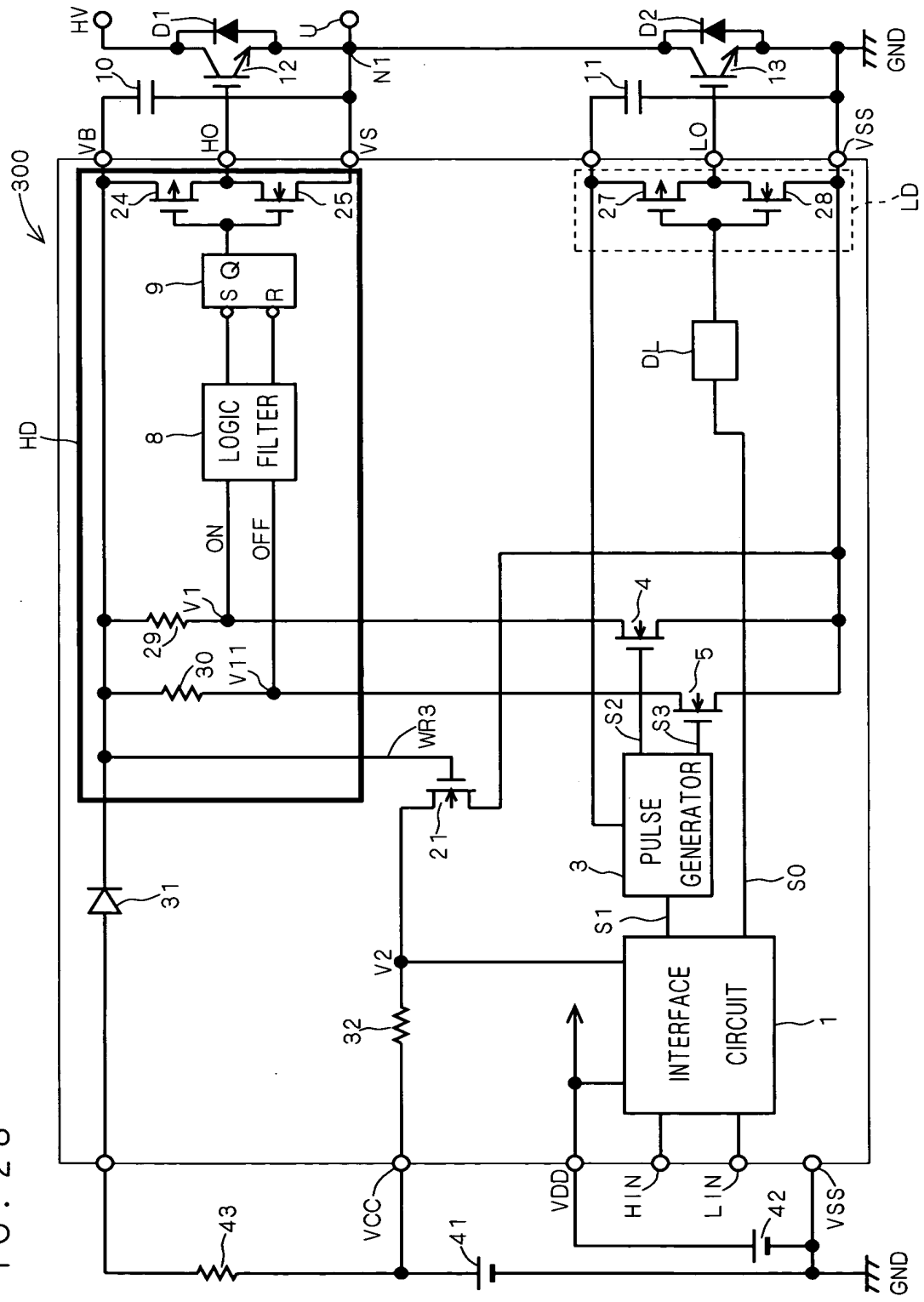


FIG. 29

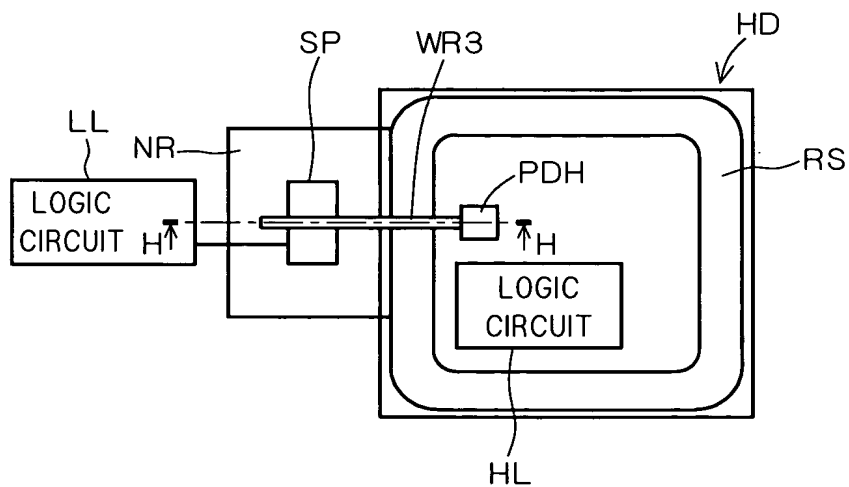


FIG. 30

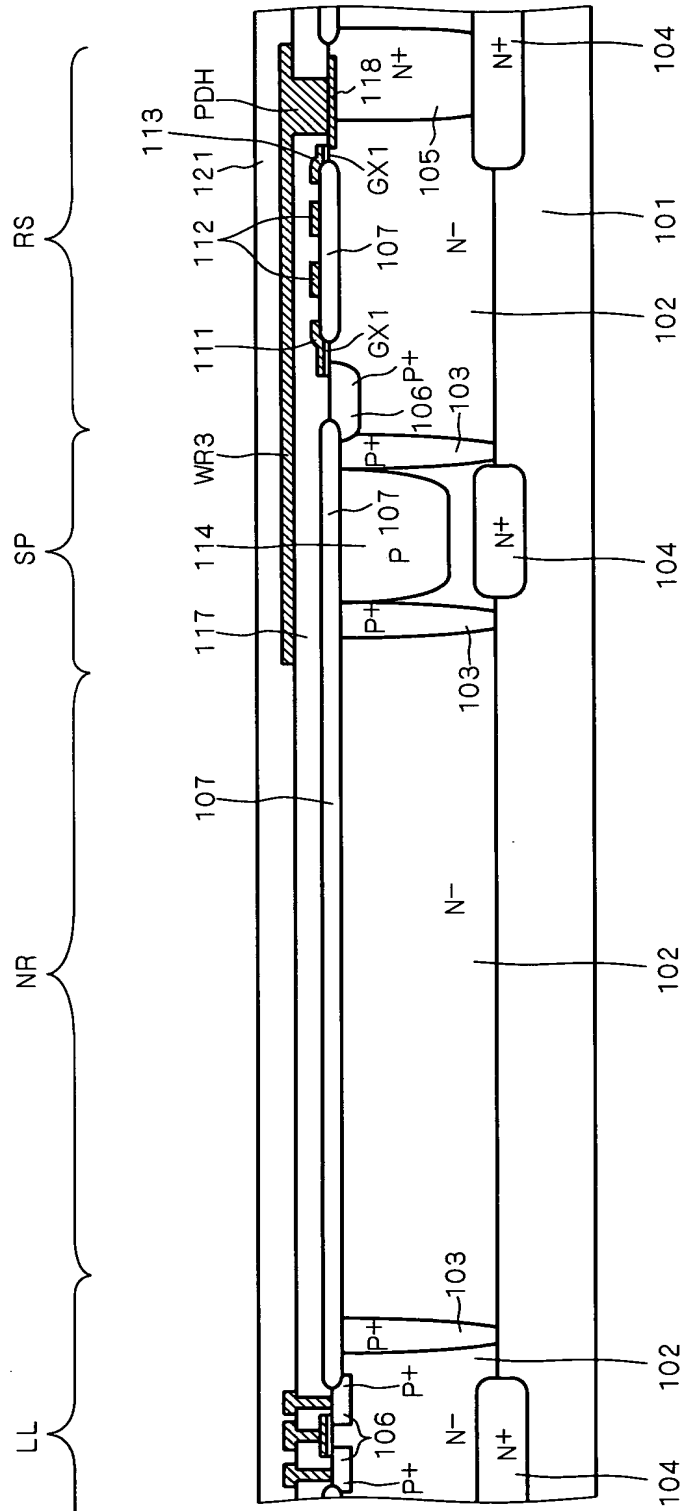


FIG. 31

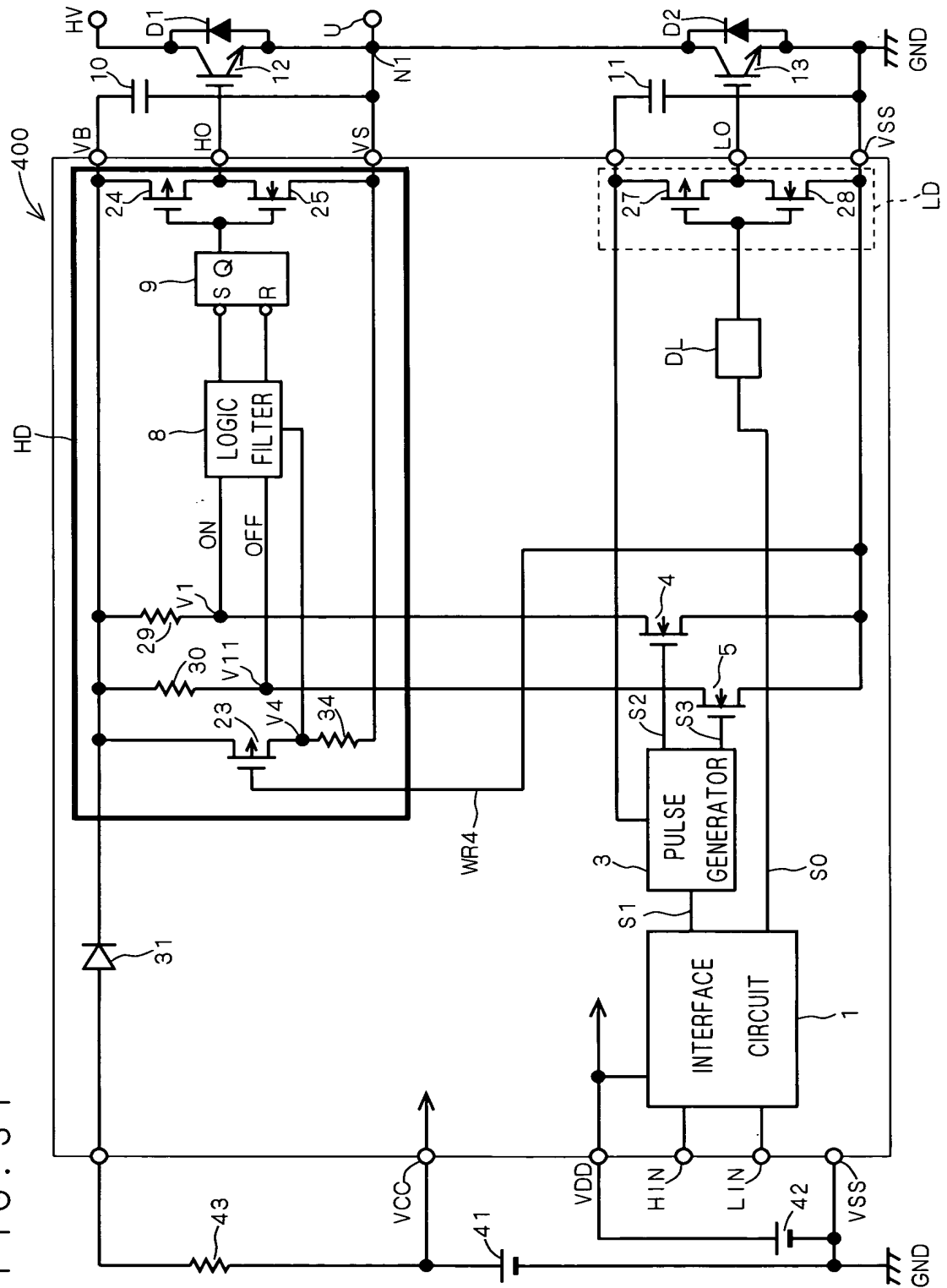
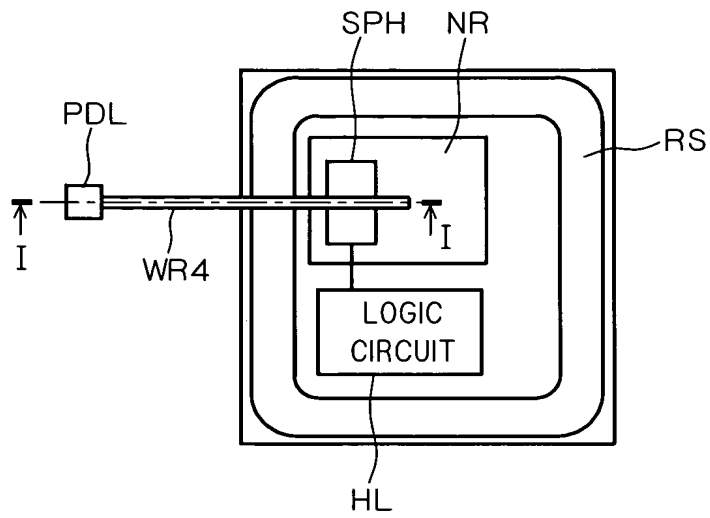


FIG. 32



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